Xedge T1/E HDCC LIM

T1/E1 High Density Cross Connect LIM

INTRODUCTION

Service providers and private network operators need flexible ways to accommodate applications that require aggregation of T1 and E1 circuits across a packet network. Applications can be as varied as leased line provisioning, remote site aggregation, metro-area network aggregation, cellular backhaul or even the bonding of T1s or E1s to enhance link bandwidth using Multi-Link Point-to-Point protocol (ML-PPP) or Inverse Multiplexing for ATM (IMA).

The Xedge T1/E1 High Density Cross Connect LIM can cost-effectively transport circuit emulated services and consolidate those circuits in higher order links over packet or cell networks. The 28/32-port LIM provides all physical interfaces, packet/cell delineation and convergence sublayers. Front panel connectors include two SFP (OC-3/12) and two DS3 or E3 line interfaces, along with 28 ports for T1 links and 32 ports for E1 links. The LIM operates in three circuit emulation modes: SAToP, CESoPSN or AAL-1. In addition to circuit emulation services, the T1/E1 HDCC LIM supports Multi-Link Point-to-Point protocol (ML-PPP), Channelized DS3 and Channelized OC-N/STM-N.

CIRCUIT EMULATION

SAToP - The LIM supports Structure Agnostic TDM over Packet (SAToP) according to RFC 4553. The RFC describes a method for encapsulating TDM bitstreams into packet. This mode of operation is for clear channel only.

CESoPSN - The LIM supports Circuit Switch Circuit Emulation Service over a Packet Switched (CESoPSN) network in accordance with RFC 5086. This mode of operation provides for NxDS0 signals as pseudowires over packet switched networks.

AAL-1 - The LIM supports AAL-1 ATM circuit emulation in accordance with ATM Forum and ITU standards, where the LIM operates in structured and clear channel modes.

DS0, DS1/E1, DS3/E3, OC3/STM1 MAPPING

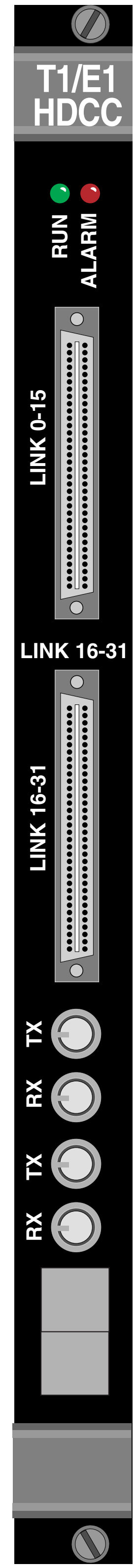
The T1/E1 HDCC LIM provides flexible mapping of T1s and E1s for consolidation in PDH and SDH facilities (T3s, E3s, OC-3/OC12/STM1/STM4).

Channelized DS3/E3 - The LIM provides channelized DS3 capability via two onboard DS3/E3 ports. Twenty-eight T1s can be aggregated into DS3. The LIM enables an integral DS0 cross-connect function as well mapping of DS1s to DS3s.

Channelized OCN - The LIM supports channelized OC-N. Two on board OC-N ports are available on the HD LIM. A single OC3 can support 63 E1s or 84 T1s.

LIM HIGHTLIGHTS

- Single-slot module provides 28/32 ports of DS1/E1 for Circuit Emulation Services (CES)
- Channelized circuit emulation support (CESoPSN-RFC 5086) and AAL1
- Clear Channel Circuit Emulation (SAToP RFC4553 or AAL1)
- ANSI T1.102, T1.107, T1.403, T1.408, ITU-T G.703, G.704
- Configured E1 ports conform to ITU-T G.703, G.704
- Provides two DS3/E3 ports
- Provides one OC3/OC12-STM1/STM4 port with an additional port for automatic protection switching.
- On-board support for multiplexed DS1 to DS3 (M13); DS3<->DS1<->nxDS0
- SDH E3 mapping
- SONET DS3 mapping
- DS0, DS1/E1, DS3/E3, OC3/STM1 Mapping
- Support for channelized OC12/STM4
- Multi-link Bundling on T1/E1 channels
- Support for Multi-Link Point-to-Point Protocol (ML-PPP) - RFC 1990
- Pseudowire Emulation (PWE)
- Interworking function with Ethernet support
- Managed via RS232 console port, remote inband Telnet, SNMP, Ethernet, and ProSphere NMS.
- Transmit timing options for each port: System, Adaptive, External or Local Oscillator (internal). Local oscillator supports failover scenarios.
- Conforms to IEEE 1588 Precision Timing Protocol Version 2 as an IEEE 1588 Client over Ethernet.
- Designed for use with the PCX controller in any Xedge switch chassis
- Front panel LEDs indicate In Service, Alarm and Loopback status.



Multi-Link Point-to-Point Protocol

Xedge T1/E1 HDCC supports the Point-to-Point protocol over T1s or E1s that are grouped together to form a bandwidth higher than 1.54 Mbps (T1) or 2 Mbps (E1). Grouping T1 or E1 circuits is a flexible means of creating higher bandwidth on a link costing less than a full DS3 or E3 circuit. The largest T1 group is 28; the largest E1 group is 32.

For example, four E1s can be bonded to created 4 x 2M or 8 megabits on a link. The LIM can provide multiple subgroups of up to 32 T1s or E1s in a bonded group. Subgroups of less than eight T1s or E1s are also supported.

Inverse Multiplexing for ATM (IMA)

Xedge T1/E1 HDCC supports Inverse Multiplexing for ATM. The IMA feature allows for the transmission of ATM cells grouped together to create higher bandwidth on a link. Up to 28 T1 ports or 32 E1 ports can be bonded in a group. Alternatively multiple sub-groups can be bonded, or single T1s or E1s can be provisioned for service. IMA implementation in the LIM complies with the ATM Inverse Multiplexing for ATM standard.

Flexible, Scalable Operation

An important feature aspect of the T1/E1 High Density Cross Connect LIM is that the user ingress (and trunk egress) Ethernet capacity traffic can grow as additional user needs grow. The LIM installs behind the Xedge PCX slot controller, a high capacity multiservice engine supporting VLAN, IP, Ethernet, MPLS, and ATM. Low-, mid- and high-density Xedge chassis options allow efficient sparing and scalability. The 1RU Xedge 6002 chassis supports 56 ports (2x28 T1 or 2x32 E1 ports), while the highest density Xedge 6640/6645 switches can support up to 392 T1 or 442 E1 ports.

Timing Options

The Xedge T1/E1 HDCC LIM provides node timing/synchronization in compliance with IEEE 1588. It also supports applications where individually configured port timing must be maintained across a packet network in accordance with ITU-T G.8261/RFC 4197. Each link can be optioned to one of four transmit timing modes:

- With System timing the LIM employs the Xedge switch timing bus structure, selecting which timing bus to use as the 8KHz reference to generate timing for the LIM.
- With an External clock reference, timing is derived from other links on the LIM.
- With the Local Oscillator on the LIM (an independent clock reference) timing is generated for the LIM.

With the Adaptive clock reference on the LIM, when there are cell/packet arrival rate changes, this clock also changes. It will then clock the transmit timing for the link on the LIM to adapt to the new derived clock. Each of the 28 T1 and 32 E1 ports can use different derived timing.

Fig. 1: Front panel features of the Xedge T1/E1 HDCC LIM

Fig. 2: The LIM providing T1 or E1 ports for circuit emulation services over a packet network over Ethernet

Fig. 3: A typical channelized D3 application with the M1:3 multiplexing function over a PDH network

Fig. 4: Typical channelized OC-N/STM-N application over packet

Fig. 5: The LIM grouping T1/E1 circuits in an ML-PPP application where Ethernet connectivity is not available

Figure 2
T1/E1 CES Aggregation

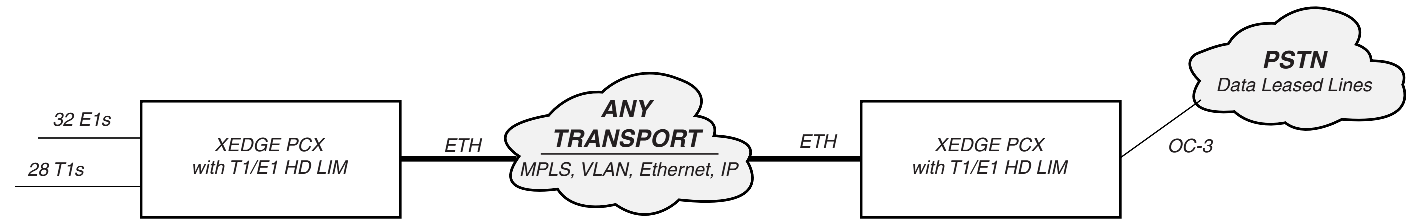
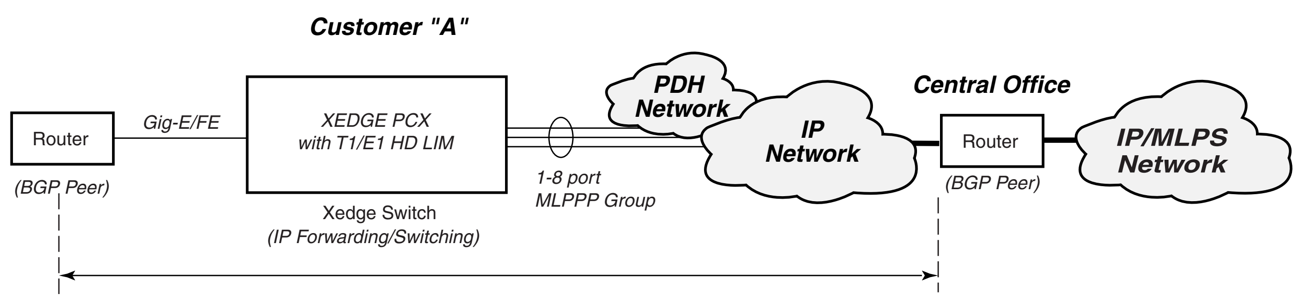


Figure 3
Channelized DS3-M13 with NxDS0

Figure 4
Channelized STM-1 with NxDS0

Figure 5
Multi-Link Point-to-Point Protocol Application



Xedge T1/E HDCC LIM

Physical Specifications

Xedge PCX Slot Controller only (Dual-slot Module)

(Horizontally installed)
Dual-slot Height: 40.13 mm (1.58 in.)
Width: 395.73 mm (15.58 in.)
Depth: 240.53 mm (9.47 in.)
Weight: TBD

Xedge T1/E1 HD Line Interface Module

Width: 19.81 mm (0.78 in.)
Height: 261.62 mm (10.3 in.)
Depth: 198.12 mm (7.80 in.)
Weight: TBD

Xedge PCX and LIM in Xedge 6002 Chassis

Width: 482.61 mm (19.0 in.)
Height: 40.38 mm (1.59 in.)
Depth: 482.6 mm (19.0 in.)
Weight: TBD

Environmental Specifications

Non-Operating

Temperature: -40 to 70 degrees C (-40 to 158 degrees F)
Relative Humidity: Up to 95%
Altitude: up to 12,191 m (40,000 ft)

Operating

Temperature: 0 to 50 degrees C (32 to 122 degrees F)
Relative Humidity: Up to 95% non-condensing
Altitude: -60 to 4,0000 m (-197 to 13,123 ft)

Electrical Specifications

Dependent on Xedge Chassis used:
- Xedge 6645 Switch Chassis (16 I/O slots, DC Power)
- Xedge 6640 Switch Chassis (16 I/O slots, AC Power)
- Xedge 6280 Switch Chassis (7 I/O slots, AC or DC Power)
- Xedge 6160 Switch Chassis (4 I/O slots, AC or DC Power)
- Xedge 6002 Switch Chassis (2 I/O slots, AC or DC Power)

Operational Specifications

Port Capacity: 28 T1 ports or 32 E1 ports

Transmit Timing Modes: System, External, Adaptive, Local Oscillator

Compatible Controllers: PCX

Network Management: SNMP

Line Encoding: B8ZS, AMI, HDB3

Performance Monitoring:
Errored Seconds, Severely Errored Seconds, Unavailable Seconds

Transmit Timing Modes:
System clock, Adaptive clock, External clock or Internal oscillator

Standard Interfaces

DS1/ E1 Services:
T1/E1 ANSI T1.102, T1.107, T1.403, T1.408, ITU-T G.703, G.704

DS3 Services:
ANSI T1.102, T1.107, T1.646, T1.408, ITU-T G.703, G.804

E3 Services:
ITU-T G.703, G.804, G.751, G.832, ITU-T1.452

OCN Services:
ANSI T1.105, ITU-T G.702, G.703, G.704, GR-253-CORE

Management:
SNMP, standard and GDC MIB management, and GDC's ProSphere Network Management System

IPV6 Addressing:
Conforms to RFC 1884 IPV6 addressing schemes

Diagnostics & Alarms

Diagnostics: Transmit, Receive, and Payload Loopbacks

Status LEDs:
IS (In Service); LS (Loss of Signal); AL (Loopback or Loss of Frame)

Alarms:
IS (In Service); LS (Loss of Signal); AL (Loopback or Loss of Frame)

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