

ATM Cell Processing Module

Introduction to Xedge ACP

GDC's Xedge ACP is a slot controller that performs dedicated ATM cell processing functions in an Xedge switch, such as traffic management and Virtual Channel Identifier/Virtual Path Identifier (VCI/VPI) translation. Physical interfaces connect with other Xedge switches, and attach to LAN hubs, routers, PBX equipment, high performance workstations and other devices with ATM interfaces.

The Xedge ACP cell controller supports the DS1 (T1), DS3 (T3), E1, and E3 PDH Physical Layer interfaces, and HSSI, LCE-16 and serial I/O interfaces. Up to two ingress/egress data paths and up to 16 ingress data paths are supported per controller.

There are four models of the Xedge ACP controller that offer distinct ingress/egress cell buffer sizes:

- 4K cells ingress/4K egress
- 16K cells ingress/16K egress
- 16K cells ingress/64K egress
- 64K cells ingress/64K egress

System Compatibility

The Xedge ACP plugs into a single slot of an Xedge AC- or DC-powered shelf: Xedge 6160 (4 slots), Xedge 6280 (7 slots) or the 16-slot Xedge 6640/6645 shelves.

The Xedge ACP is intended for use with any one of the following Enhanced Clocking LIMs:

- Xedge DS1-2CS or DS1-4C LIM for T1 circuits.
- Xedge E1-2CS or E1-4C LIM for E1 circuits
- Xedge DS3 LIM for DS3 circuits
- Xedge E3 LIM for E3 circuits
- Xedge LCE-16 for legacy circuit emulation
- Xedge HSSI-DTE for high speed DTE serial circuits
- Xedge SI-2C, SI-4C or Xedge ASIO LIM for serial circuits (RS442, RS449, EIA/TIA-530, V.35, X.21)

Diagnostics

Diagnostics are provided via status LEDs for all ports, diagnostic screens for all faults, and Local and Line Loopbacks. Management Interfaces include:

- Standard SNMP
- MIB management
- GDC's ProSphere Network Management System

Feature Highlights

- High performance ATM cell switching with advanced modular buffering for up to 256,000 cells per controller.
- Supports T1/E1, DS3/E3, HSSI or serial circuits.
- Supports ATM Multicast
- Selectable transmit clock: System, Local Oscillator or Local Link
- Low Priority FIFO buffering can be tailored to match network profiles via three threshold parameters.
- Provides Diagnostic, Line, Payload, and Cell Loopback Tests.
- Meets ATM Forum UNI 3.1 for traffic management.
- Secure configuration and management via SNMP or MIB editor over Telnet/craft connection, or via ProSphere Network Management System.

Low Priority Buffering

As high priority traffic increases, the ACP can buffer low priority traffic until bandwidth becomes available. For the available buffer size, three threshold parameters can be set in 1K cell increments to tailor the Low Priority Buffer to match traffic profiles:

- EFCI threshold (Explicit Forward Congestion) indicates approaching congestion.
- CLP=1 threshold at which low priority traffic of CLP=1 begins to be discarded.
- Logical Buffer Size threshold sets the size at which the Low Priority Buffer operates.

As low priority buffering is increased, more low priority traffic finds space available in the bit stream. By adjusting buffer thresholds, a tolerable cell delivery delay rate for low priority traffic can be achieved.

Compliance

Xedge ACP supports the Plesiochronous Digital Hierarchy (PDH) which comprises the various bit rates defined by the ITU-T in 1972 for North America, Europe and Japan. ATM cells are transported in PDH frames according to the ITU-T Recommendation G.804. The Xedge ACP cell controller also meets ATM Forum UNI 3.1 for traffic management.

